United States Patent and Trademark Office

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,607	12/29/2003	James S. Song	TI-35767 (032350.B545)	8925

23494	7590	10/23/2006

EXAMINER
SUGENT, JAMES F

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/750,607	SONG ET AL.
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**.　　　2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received August

15, 2006 for application number 10/750,607 originally filed December 29, 2003. The Office

5   hereby acknowledges receipt of the following and placed of record in file: amended claims 1-20

are submitted for examination.

Claim Rejections - 35 USC § 103

10   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

15

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

20   U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness
25   or nonobviousness.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al.

(U.S. Patent No. 6,549,045 B1) (hereinafter referred to as Wang) in view of Cheung et al. (U.S.

Patent No. 6,564,329 B1) (hereinafter referred to as Cheung).

As to claim 1, Wang discloses a delay equalizer (clock channel 20) for balancing clock

signals in a clock tree (Wang discloses a clock system wherein said system provides multiple

clocks with low skew and proper alignment; column 2, lines 5-15 and column 4, lines 17-21),

comprising: a register (flip-flop 110) operable to: receive (as shown in figure 2) a divided input

5   clock signal (105) (Wang discloses the flip-flop [110] receiving M-bit clock signals provided

from a bit string within a shift register [100] thus producing a divided frequency; column 2, lines

35-43 and column 4, lines 40-58 and column 5, lines 52-63 and column 6, lines 40-44); receive

(as shown in figure 2) a non-divided input clock signal (Wang discloses the flip-flop [110]

receiving an undivided input clock signal [50] to drive the flip-flop; column 4, lines 40-58); and

10   generate a first output clock signal (115) based on the received divided input clock signal (105)

and the received non-divided input clock signal (50), the first output clock signal being

associated with a first delay (Wang discloses the flip-flop [110] receiving signals 50 and 105

through a delay [D-type] flip-flop and thus producing a delayed output signal [115] that is

delayed secondary to the propagation of the signals through the flip-flop; column 4, lines 47-58

15   and column 5, lines 19-23); a delay line (delay circuit 120) operable to: receive (as shown in

figure 2) the non-divided input clock signal (50) (column 4, lines 63-67); delay the non-divided

input clock signal for a time substantially equivalent to the first delay associated with the first

output clock signal (Wang discloses the signals produced by 110 and 120 [signals 115 and 125]

being matched and therefore having equal delays; column 5, lines 14-30); and generate a second

20   output clock signal (125) being associated with a second delay substantially equal to the first

delay of the first output signal (column 4, lines 63-67 and column 5, lines 14-30); and a

multiplexer (multiplexer circuit 130) operable to: receive (as shown in figure 2) the first output

clock signal (115) and the second output clock signal (125) (column 5, lines 1-3); receive (as

shown in figure 2) a select control signal (MUXADR signal) indicating which of the first output

clock signal or the second output clock signal to select (column 5, lines 4-13); select either the

received first output clock signal (115) or the second output clock signal (125) based on the

5   select control signal (column 5, lines 4-13); and generate the selected first output clock signal

(115) or second output clock signal (125) as a substantially balanced third output clock signal

(output 135) (Wang discloses the output signal from the multiplexer [130] being a matched

signal since the inputs to the multiplexer are matched and therefore balanced; column 5, lines 1-7

and column 5, lines 19-30 and column 8, line 53 thru column 9, line 13).

10   Wang does not disclose the select control signal is programmable on the fly, and wherein

the select control signal is constrained to avoid errors in clock distribution.

            Cheung teaches a dynamic clock distribution circuit (312) that is capable of providing

various clock frequencies that can be selected (via MUX selection signal) during run-time

(dynamically on the fly) (column 2, lines 27-30 and column 3, lines 22-24 and column 6, lines

15   column 7, lines 41-55 and column 9, lines 15-30). Cheung further teaches the request lines used

for clock selection are synchronized to the adder used for selecting the divided clock therefore

constrained to avoid errors (column 8, lines 17-33). Cheung further teaches the additional benefit

of power conservation (column 2, lines 20-25).

            It would have been obvious to one of ordinary skill of the art having the teachings of

20   Wang and Cheung at the time the invention was made, to modify the clock selection signal of

Wang to include the ability of having the select control signal as programmable on the fly in

addition to the select control signal being constrained to avoid errors as taught by Cheung. One

of ordinary skill in the art would be motivated to make this combination of having the select

control signal as programmable on the fly in addition to the select control signal being

constrained to avoid errors in view of the teachings of Cheung, as doing so would give the added

benefit of power conservation (as taught by Cheung above).

5   As to claim 2, Wang in combination with Cheung taught the delay equalizer in claim 1,

as shown above. Wang further discloses the delay equalizer wherein: the divided clock in signal

being associated with a functional mode (channel) of a device (10) comprising the delay

equalizer (Wang discloses clock output signals being selectable parameters within the circuit

utilizing the divided/undivided clock balancing scheme; column 4, lines 7-39); and the select

10   control signal (MUXADR) received by the multiplexer (130) comprises a divided/non-divided

select control signal (column 5, lines 4-13); the delay equalizer (20) is operable to substantially

balance the input clock signal between one or more functional modes of the device (Wang

discloses all of the possible output paths being matched with minimal skew and therefore

balanced; column 4, lines 33-39).

15   As to claims 3 and 4, they are directed to the delay equalizer of steps set forth in claim 2.

Therefore, they are rejected for the same basis as set forth hereinabove.

        As to claim 5, Wang in combination with Cheung taught the delay equalizer in claim 1,

as shown above. Wang further discloses the delay equalizer wherein the delay equalizer is

associated with a clock-gating cell and is operable to provide the substantially balanced third

20   output clock signal to the clock-gating cell as an input clock signal to the clock-gating cell such

that an output clock signal generated by the clock-gating cell is substantially balanced (As is

known in the art, a clock tree synthesis tool can be applied to balance all the clocks throughout

the system and therefore necessitates clock gates to select a desired clock, whether divided or

undivided, dependent on control signals used by said synthesizers; column 1, line 26 thru column

2, line 2).

As to claim 6, Wang in combination with Cheung taught the delay equalizer in claim 1,

5   as shown above. Wang further discloses the delay equalizer wherein: the register comprises a

flip-flop register (110) (column 4, lines 40-44); and the delay line (120) comprises one or more

buffers for delaying the non-divided clock signal (Wang discloses the delay circuit in comprising

inverter buffers [305, 310, 330 and 335]; column 8, lines 53-63).

As to claim 7, Wang discloses a method for balancing clock signals in a node (channel)

10   of a clock tree (column 2, lines 5-34), comprising: receiving a divided input clock signal (via

signal 105 from shift register 100) at a register (flip-flop 110) (Wang discloses the flip-flop [110]

receiving M-bit clock signals provided from a bit string within a shift register [100] thus

producing a divided frequency; column 2, lines 35-43 and column 4, lines 40-58 and column 5,

lines 52-63 and column 6, lines 40-44); receiving a non-divided input clock signal (via signal 50)

15   at the register (flip-flop 110) (Wang discloses the flip-flop [110] receiving an undivided input

clock signal [50] to drive the flip-flop; column 4, lines 40-58); generating at the register (via

signal 115) a first output clock signal based on the received divided input clock signal (105) and

the received non-divided input clock signal (50), the first output clock signal (115) being

associated with a first delay (Wang discloses the flip-flop [110] receiving signals 50 and 105

20   through a delay [D-type] flip-flop and thus producing a delayed output signal [115] that is

delayed secondary to the propagation of the signals through the flip-flop; column 4, lines 47-58

and column 5, lines 19-23); receiving the non-divided input clock signal (50) at a delay line

(delay circuit 120) (column 4, lines 63-67); delaying at the delay line the non-divided input clock

signal for a time substantially equivalent to the first delay associated with the first output clock

signal (Wang discloses the signals produced by 110 and 120 [signals 115 and 125] being

matched and therefore having equal delays; column 5, lines 14-30); generating at the delay line

5   (120) a second output clock signal (120) being associated with a second delay substantially equal

to the first delay of the first output signal (Wang discloses the signals produced by 110 and 120

[signals 115 and 125] being matched and therefore having equal delays; column 5, lines 14-30);

receiving at a multiplexer (130) the first output clock signal (via signal 115) and the second

output clock signal (via signal 125) (column 5, lines 1-3); receiving at the multiplexer a select

10   control signal (MUXADR signal) indicating which of the first output clock signal or the second

output clock signal to select (column 5, lines 4-13); selecting at the multiplexer either the

received first output clock signal (115) or the second output clock signal (125) based on the

select control signal (MUXADR signal) (column 5, lines 4-13); and generating the selected first

output clock signal (115) or second output clock signal (125) as a substantially balanced third

15   output clock signal (output 135) (Wang discloses the output signal from the multiplexer [130]

being a matched signal since the inputs to the multiplexer are matched and therefore balanced;

column 5, lines 1-7 and column 5, lines 19-30 and column 8, line 53 thru column 9, line 13).

Wang does not disclose the select control signal is programmable on the fly, and wherein

the select control signal is constrained to avoid errors in clock distribution.

20   Cheung teaches a dynamic clock distribution circuit (312) that is capable of providing

various clock frequencies that can be selected (via MUX selection signal) during run-time

(dynamically on the fly) (column 2, lines 27-30 and column 3, lines 22-24 and column 6, lines

column 7, lines 41-55 and column 9, lines 15-30). Cheung further teaches the request lines used

for clock selection are synchronized to the adder used for selecting the divided clock therefore

constrained to avoid errors (column 8, lines 17-33). Cheung further teaches the additional benefit

of power conservation (column 2, lines 20-25).

5   It would have been obvious to one of ordinary skill of the art having the teachings of

Wang and Cheung at the time the invention was made, to modify the clock selection signal of

Wang to include the ability of having the select control signal as programmable on the fly in

addition to the select control signal being constrained to avoid errors as taught by Cheung. One

of ordinary skill in the art would be motivated to make this combination of having the select

10   control signal as programmable on the fly in addition to the select control signal being

constrained to avoid errors in view of the teachings of Cheung, as doing so would give the added

benefit of power conservation (as taught by Cheung above).

          As to claim 8, Wang in combination with Cheung taught the method in claim 7, as shown

above. Wang further discloses the method wherein: the divided clock in signal being associated

15   with a functional mode (channel) of a device (10) comprising the delay equalizer (Wang

discloses clock output signals being selectable parameters within the circuit utilizing the

divided/undivided clock balancing scheme; column 4, lines 7-39); and the select control signal

(MUXADR) received by the multiplexer (130) comprises a divided/non-divided select control

signal (column 5, lines 4-13); the method substantially balancing the input clock signal between

20   one or more functional modes of the device (Wang discloses all of the possible output paths

being matched with minimal skew and therefore balanced; column 4, lines 33-39).

As to claims 9 and 10, they are directed to the methods of steps set forth in claim 8.

Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 11, Wang in combination with Cheung taught the method in claim 7, as

shown above. Wang further discloses the method further comprising providing the substantially

5   balanced third output clock signal to a clock-gating cell as an input clock signal to the clock-

gating cell such that an output clock signal generated by the clock-gating cell is substantially

balanced (As is known in the art, a clock tree synthesis tool can be applied to balance all the

clocks throughout the system and therefore necessitates clock gates to select a desired clock,

whether divided or undivided, dependent on control signals used by said synthesizers; column 1,

10   line 26 thru column 2, line 2).

As to claim 12, Wang in combination with Cheung taught the method in claim 7, as

shown above. Wang further discloses the method wherein: the register comprises a flip-flop

register (110) (column 4, lines 40-44); and the delay line comprises one or more buffers for

delaying the non-divided clock signal (Wang discloses the delay circuit in comprising inverter

15   buffers [305, 310, 330 and 335]; column 8, lines 53-63).

Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al.

(U.S. Patent Publication No. 2003/0135836 A1) (hereinafter referred to as Chang) in view of

Nadeau-Dostie et al. (U.S. Patent Publication No. 2003/0146777 A1) (hereinafter referred to as

Nadeau-Dostie).

20   As to claim 13, Chang disclose a method for balancing one or more clock signals in a

clock tree having a clock distribution (paragraph 37), comprising: associating a first delay

equalizer (48 and 49 at and above enable points C2 and C3) with at least one of a plurality of

clock-gating cells (51 and 52) arranged in one or more levels in the clock tree (as shown in Fig.

8), the first delay equalizer operable to provide a balanced input clock signal to the clock-gating

cell such that an output clock signal generated by the clock-gating cell is substantially balanced

(paragraphs 36-39); a second delay equalizer (48 and 49 at and below enable points C2 and C3)

5   operable to substantially balance the one or more clock signals (paragraphs 36-39); extracting a

common clock distribution topology from the clock tree, the topology accounting for

substantially all paths of the topology (paragraph 39); determining one or more clock paths

(subtrees) to be balanced (Chang discloses determining which subtree paths need to be re-

evaluated in order to properly balance the entire tree; paragraphs 43); analyzing any local clock

10   paths that were left out of the common clock distribution topology (Chang discloses creating new

endpoints in the clock subtree structures to properly evaluate and determine a balanced subtree

by inserting new buffers to balance the delays; if the subtree is not balanced, a new endpoint is

determined thus re-evaluated thus discovering new subtree branches that were left out of the

evaluation process before; paragraphs 44-45); developing a local balancing strategy (subtree

15   synthesis) for the local clock paths that were left out of the common clock distribution topology

to determine one or more constraints for substantially balancing the local clock paths (Chang

discloses balancing the lower subtrees and combining [synthesizing] all of the subtrees using two

techniques [zero-skew algorithm and subtree compression process] and re-evaluating until all

subtrees are balanced; paragraphs 52-54); combining (synthesizing) the local balancing strategy

20   (subtree analysis) with the common clock distribution (starting at the lower levels and working

upward to all levels of the tree) to form a clock tree synthesis constraint to substantially balance

the common clock distribution topology and the local clock paths in a substantially automatic

process (Chang discloses balancing all levels of the tree using the CTS algorithm that automatically loops through a balancing/synthesizing process until the entire tree is synthesized; paragraphs 47-50).

Chang does not disclose the system: wherein the clock balancing system has multi-mode

5   clock distribution; wherein the second delay equalizers are each associated with one or more clock-dividing and selection modules; wherein balanced clock signals associated with the second delay equalizers are between two or more functional modes; the common clock distribution topology accounting for substantially all of modes and clock-dividing paths of the topology; and, the determining of the one or more clock paths to include each comprising a multi-mode

10   dependant clock path, wherein the multi-mode dependent clock path includes the two or more functional modes.

Nadeau-Dostie teaches clock controlling circuitry (12) that balances multiple clocks (CLKA and CLKB): wherein the clock balancing system has multi-mode clock distribution (normal operating mode and test mode; paragraphs 5 and 39-43); wherein the second delay

15   equalizers are each associated with one or more clock-dividing and selection modules (prescalars 64 and 66 in addition to MUXes 60, 62 and 68; paragraphs 21 and 22); and, wherein balanced clock signals associated with the second delay equalizers are between two or more functional modes (Nadeau-Dostie teaches the prescalars being selected dependent on the mode selection; paragraphs 21 and 22). Nadeau-Dostie has the additional feature of facilitating the distribution of

20   clock signals to various clock domains and cores during both normal mode and testing mode which in turn will assist in the synchronization at all levels of the testing (paragraph 3, lines 21 thru paragraph 5).

It would have been obvious to one of ordinary skill of the art having the teachings of

Chang and Nadeau-Dostie at the time the invention was made, to modify the system of Chang to

include multi-mode clock balancing within the clock distribution wherein clock dividing circuits

are used and balanced within the tree as taught by Nadeau-Dostie such that the extracting,

5   balancing and combination processes of Chang account for multi-modal analysis and balancing.

One of ordinary skill in the art would be motivated to make this combination of having multi-

mode clock balancing within the clock distribution wherein clock dividing circuits are used and

balanced within the tree in view of the teachings of Nadeau-Dostie, as doing so would give the

added benefit of facilitating the distribution of clock signals to various clock domains and cores

10   during both normal mode and testing mode which in turn will assist in the synchronization at all

levels of the testing (as taught by Nadeau-Dostie above).

As to claim 14, Chang in combination with Nadeau-Dostie taught the method in claim 13,

as shown above. Chang further teaches the method wherein determining the one or more clock

paths to be balanced comprises: determining an impact that balancing a particular clock path

15   would have on overall clock tree balance and performance of a device associated with the clock

tree (paragraph 43); determining whether the determined impact of the particular clock path

exceeds a predetermined impact (paragraph 45, lines 1-8); and if it is determined that the

determined impact of balancing the particular clock path exceeds the predetermined impact,

determining that the particular clock path should be balanced (paragraph 45).

20   As to claim 15, it is directed to the method of steps set forth in claim 14. Therefore, it is

rejected for the same basis as set forth hereinabove.

As to claim 16, Chang in combination with Nadeau-Dostie taught the method in claim 13, as shown above. Nadeau-Dostie further teaches the method comprising one or more exclusive-NOR (XNOR) gates (98, 100, 102) inserted throughout the clock tree to balance one or more portions of the clock tree, each XNOR gate operable to: receive an input clock signal on an input

5   clock path (as shown in Fig. 5); receive a test mode signal on a test mode path (as shown in Fig. 5); and generate an output clock signal on an output clock path based on an XNOR operation, a delay from the input clock path to the output clock path being independent of a delay from the test mode path to the output clock path (Nadeau-Dostie teaches logic gates [98, 100, 102] being used to determine the mode of operation; paragraph 50).

10   As to claim 17, it is directed to the method of steps set forth in claim 16. Therefore, it is rejected for the same basis as set forth hereinabove.

As to claim 18, Chang teaches a system for balancing one or more clock signals in a clock tree having a clock distribution (paragraph 37), comprising: one or more first delay equalizers (48 and 49 at and above enable points C2 and C3) each associated with at least one of

15   a plurality of clock-gating cells (51 and 52) arranged in one or more levels in the clock tree (as shown in Fig. 8), each first delay equalizer operable to provide a balanced input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced (paragraphs 36-39); one or more second delay equalizers (48 and 49 at and below enable points C2 and C3) each second delay equalizer is operable to substantially

20   balance the one or more clock signals (paragraphs 36-39); the first and second delay equalizers substantially balancing the one or more clock signals in the clock tree (paragraph 36).

Chang does not disclose the system: wherein the clock balancing system has multi-mode

clock distribution; wherein the second delay equalizers are each associated with one or more

clock-dividing and selection modules; and, wherein balanced clock signals associated with the

second delay equalizers are between two or more functional modes.

5   Nadeau-Dostie teaches clock controlling circuitry (12) that balances multiple clocks

(CLKA and CLKB): wherein the clock balancing system has multi-mode clock distribution

(normal operating mode and test mode; paragraphs 5 and 39-43); wherein the second delay

equalizers are each associated with one or more clock-dividing and selection modules (prescalars

64 and 66 in addition to MUXes 60, 62 and 68; paragraphs 21 and 22); and, wherein balanced

10   clock signals associated with the second delay equalizers are between two or more functional

modes (Nadeau-Dostie teaches the prescalars being selected dependent on the mode selection;

paragraphs 21 and 22). Nadeau-Dostie has the additional feature of facilitating the distribution of

clock signals to various clock domains and cores during both normal mode and testing mode

which in turn will assist in the synchronization at all levels of the testing (paragraph 3, lines 21

15   thru paragraph 5).

It would have been obvious to one of ordinary skill of the art having the teachings of

Chang and Nadeau-Dostie at the time the invention was made, to modify the system of Chang to

include multi-mode clock balancing within the clock distribution wherein clock dividing circuits

are used and balanced within the tree as taught by Nadeau-Dostie. One of ordinary skill in the art

20   would be motivated to make this combination of having multi-mode clock balancing within the

clock distribution wherein clock dividing circuits are used and balanced within the tree in view

of the teachings of Nadeau-Dostie, as doing so would give the added benefit of facilitating the

distribution of clock signals to various clock domains and cores during both normal mode and testing mode which in turn will assist in the synchronization at all levels of the testing (as taught by Nadeau-Dostie above).

As to claim 18, Chang in combination with Nadeau-Dostie taught the system in claim 18,

5   as shown above. Nadeau-Dostie further teaches the system comprising one or more exclusive-NOR (XNOR) gates (98, 100, 102) inserted throughout the clock tree to balance one or more portions of the clock tree, each XNOR gate operable to: receive an input clock signal on an input clock path (as shown in Fig. 5); receive a test mode signal on a test mode path (as shown in Fig. 5); and generate an output clock signal on an output clock path based on an XNOR operation, a

10   delay from the input clock path to the output clock path being independent of a delay from the test mode path to the output clock path (Nadeau-Dostie teaches logic gates [98, 100, 102] being used to determine the mode of operation; paragraph 50).

As to claim 20, it is directed to the system of steps set forth in claim 19. Therefore, it is rejected for the same basis as set forth hereinabove.

15   .

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

20   *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

5   MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

10   however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The

15   Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the

organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent

20   Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

5   James F. Sugent
      Patent Examiner, Art Unit 2116
      October 13, 2006

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100